IN THE CLAIMS:

1. (Currently Amended) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing waveforms of first output signals from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device, and for outputting fourth output signals; and

a first factor computation device directly connected to the equalization target value generation device, the first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from said first, second, and fourth output signals.

2. (Canceled)

3. (Currently Amended) The adaptive equalization circuit according to Claim [[1]] 17, wherein said first digital equalization device is an FIR filter having tap factors of a symmetric type.

4. (Canceled)

5. (Currently Amended) The adaptive equalization circuit according to Claim [[4]] 15, wherein said second digital equalization device is a FIR filter having tap factors of an asymmetric type.

6. (Canceled)

7. (Canceled)

8. (Previously Presented) The adaptive equalization circuit according to Claim 3, wherein said first factor computation device supplies the computed tap factors to the first digital equalization device and performs adaptive equalization regardless of whether phase synchronization performed by said phase synchronization device is in an unlock status.

9. (Canceled)

10. (Currently Amended) The adaptive equalization circuit according to Claim [[9]] 17, further comprising a frequency locking device for changing the frequency information to be used for computation by said interpolation position computation device so as to decrease the frequency errors detected by said frequency error monitor.

11.-14. (Canceled)

15. (New) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing waveforms of first output signals from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device, and for outputting fourth output signals;

a second digital equalization device for inputting the third output signals from said phase synchronization device and performing adaptive equalization;

a first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from said first, second, and fourth output signals; and

a second factor computation device for computing tap factors of said second digital equalization device from the third output signals from said phase synchronization device and fifth output signals from said second digital equalization device.

16. (New) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing waveforms of first output signals from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device, and for outputting fourth output signals, said equalization target value generation device comprising:

a temporary target value generation device for generating a temporary target value, that is the equalization target value of the phase-synchronized signals, and

an equalization target phase rotation device for generating a true target value, from said temporary target value, the true target value being an equalization target value before synchronizing phases by said phase synchronization device; and

a first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from said first, second, and fourth output signals

wherein said phase synchronization device is a phase synchronization loop comprising a first interpolation device for interpolating the second output signals from said first digital equalization device and an interpolation position computation device for computing an

interpolation position of said first interpolation device from sixth output signals from said first interpolation device,

said equalization target phase rotation device is a second interpolation device for interpolating said temporary target value and acquiring said true target value, an interpolation position of said second interpolation device being computed by said interpolation position computation device

said first interpolation device and second interpolation device are FIR filters, said interpolation position computation device outputs tap factors as information of the interpolation position, and if each tap factor is COE(n) where n is the number of taps, the tap factor h1 to be supplied to said first interpolation device is given by h1 = {COE(1) COE(2) COE(3) - - - COE(n)}, and

when the number of taps of said second interpolation device is the same as the number of taps of said first interpolation device, the tap factor h2 to be supplied to the second interpolation device has a symmetrical relationship with said h1, that is given by h2 = {COE(n) COE(n-1) COE(n-2) - - - COE(1)}, or the factor h2 is delayed and input to the second interpolation device,

when the number of taps of said second interpolation device is different from the number of taps of said first interpolation device, h3, that is a factor having a phase characteristic equivalent to said h1, is given by h3 = {COE(1) COE(2) COE(3) - - - COE(m)}, where m is a number of taps, and

the tap factor h4 to be supplied to said second interpolation device has a symmetrical relationship with said h3 and is given by h4 = {COE(m) COE(m-1) COE(m-2) - - - COE(1)}, or the factor h4 is delayed and input to said second interpolation device.

17. (New) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing waveforms of first output signals from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device, and for outputting fourth output signals;

a first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from said first, second, and fourth output signals; and

a frequency error monitor for monitoring frequency errors of the phase synchronization performed by said phase synchronization device, wherein when said frequency error is smaller than a predetermined value, said first factor computation device supplies computed tap factors to the first digital equalization device and starts adaptive equalization.

18. (New) An adaptive equalization circuit, comprising:

an analog-digital conversion device for sampling signals read from a recording medium;

a first digital equalization device for equalizing waveforms of first output signals from said analog-digital conversion device;

a phase synchronization device for synchronizing phases for second output signals from said first digital equalization device;

an equalization target value generation device for generating an equalization target value of said first digital equalization device from third output signals from said phase synchronization device, and for outputting fourth output signals;

a first factor computation device for receiving as input signals said first, second, and fourth output signals, and for computing tap factors of said first digital equalization device from said first, second, and fourth output signals;

a frequency information threshold device for judging frequency information of said phase synchronization device in a plurality of statuses using one or more threshold values;

a memory for storing tap factors corresponding to the statuses judged by said frequency information threshold device;

an equalization factor selection device for selecting either an output of said first factor computation device or of said memory when a tap factor is supplied to said first digital equalization device;

a status time measurement device for measuring the duration of a status of the statuses judged by said frequency information and comparing said duration with a predetermined value;

a factor computation control device for controlling the starting or stopping of the computation of said first factor computation device;

a factor memory storage processing device for transferring an instruction to stop the computation by said first factor computation device to said factor computation control device if said duration is longer than said predetermined value in said status time measurement device, and storing the tap factors after said factor computation device stops at a position corresponding to the status judged by said frequency information threshold device of said memory; and

a status change processing device for switching said equalization factor selection device so as to supply the tap factor to said first digital equalization device and notifying said factor computation control device that the computation by said first factor computation device is stopped if the tap factor corresponding to the status after change is stored in said memory when the status judged by said frequency information threshold device changes, and for switching said equalization factor selection device so as to supply the tap factor to said first digital equalization device and notifying said factor computation control device that the factor computation by said first factor computation device is started when the tap factor corresponding to the status after change is not stored in said memory.